Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.031”**

**9 8 7 6 5**

**4**

**3**

**10**

**11**

**12 13 14 1 2**

**MASK**

**REF**

**ACT32S**

**.027”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .003”**

**Backside Potential: GND**

**Mask Ref: ACT32S**

**APPROVED BY: DK DIE SIZE .027” X .031” DATE: 10/24/16**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54ACT32**

**DG 10.1.2**

#### Rev B, 7/1